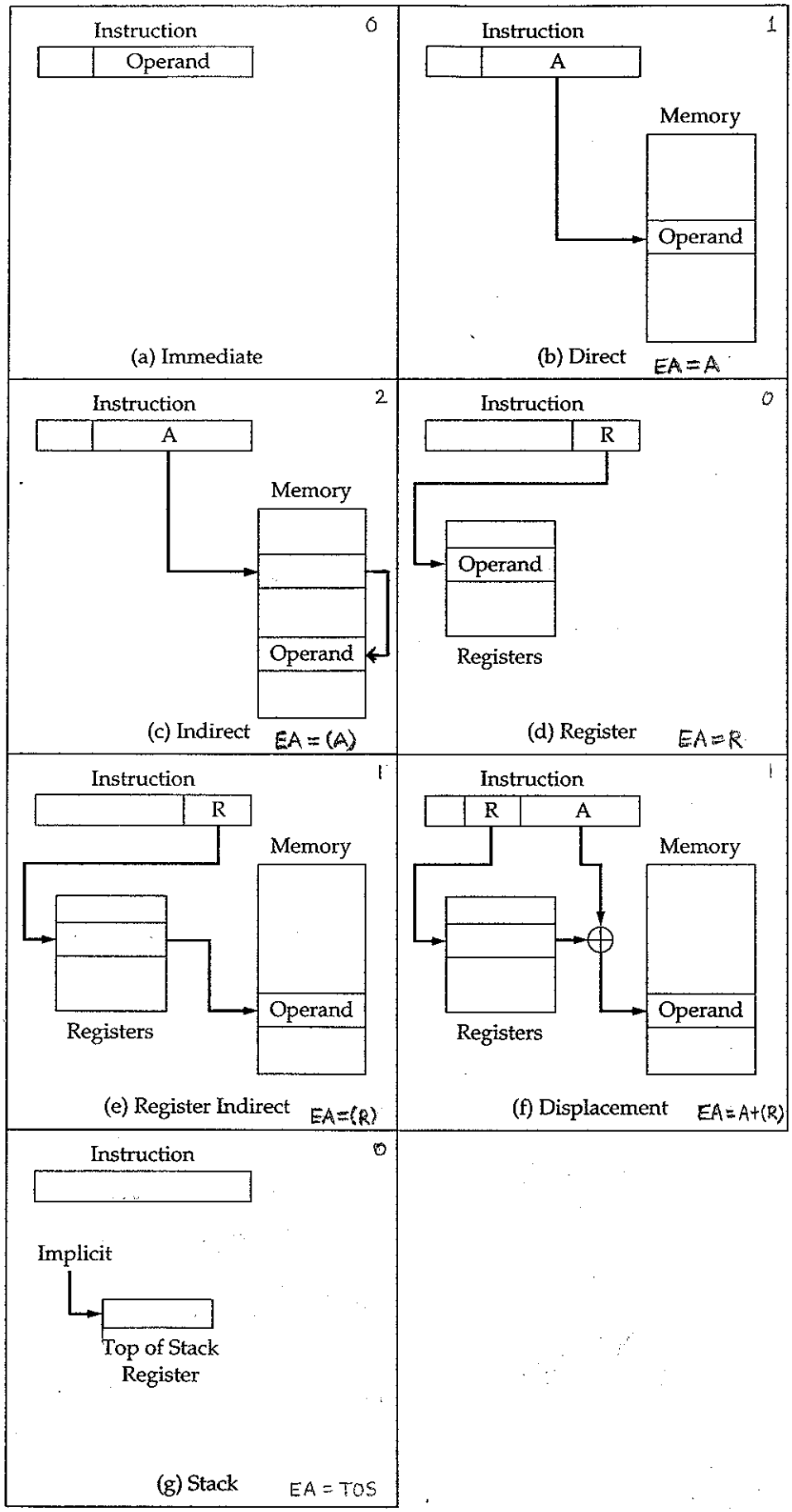


FIGURE 11.1. Addressing modes

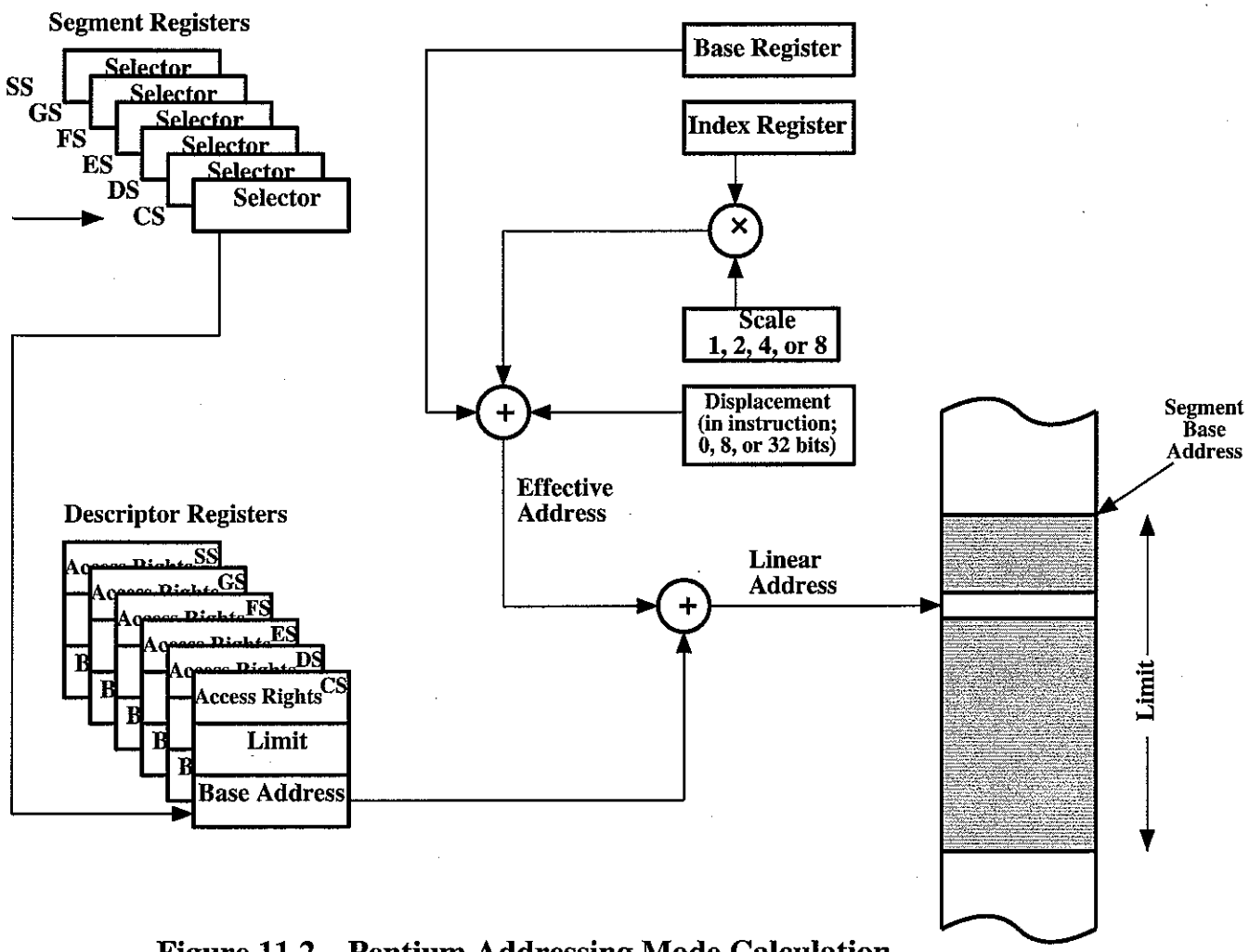


Figure 11.2 Pentium Addressing Mode Calculation

Table 11.2 Pentium Addressing Modes

Mode	Algorithm
Immediate	Operand = A
Register Operand	LA = R
Displacement	LA = (SR) + A
Base	LA = (SR) + (B)
Base with Displacement	LA = (SR) + (B) + A
Scaled Index with Displacement	LA = (SR) + (I) × S + A
Base with Index and Displacement	LA = (SR) + (B) + (I) + A
Base with Scaled Index and Displacement	LA = (SR) + (I) × S + (B) + A
Relative	LA = (PC) + A

LA	=	linear address
(X)	=	contents of X
SR	=	segment register
PC	=	program counter
A	=	contents of an address field in the instruction
R	=	register
B	=	base register
I	=	index register
S	=	scaling factor

11.3 Instruction Formats

Issues:

(1) Instruction Length

More opcodes
More operands → shorter program — Trade-off
More addressing modes → flexibility
Larger memory address range

Word size
- one character = 8 bits
- multiple of 8

Example. IBM S/360

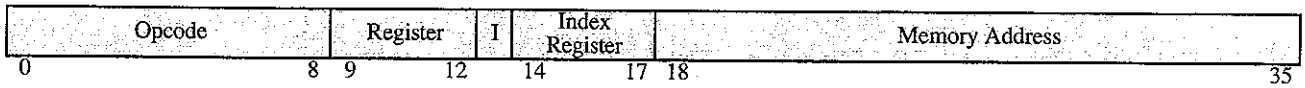
1 word = 32 bits (4 bytes)
1 half word = 2 bytes
1 double word = 8 bytes

Note. IBM 700/7000 series: 36 bits

(2) Allocation of bits

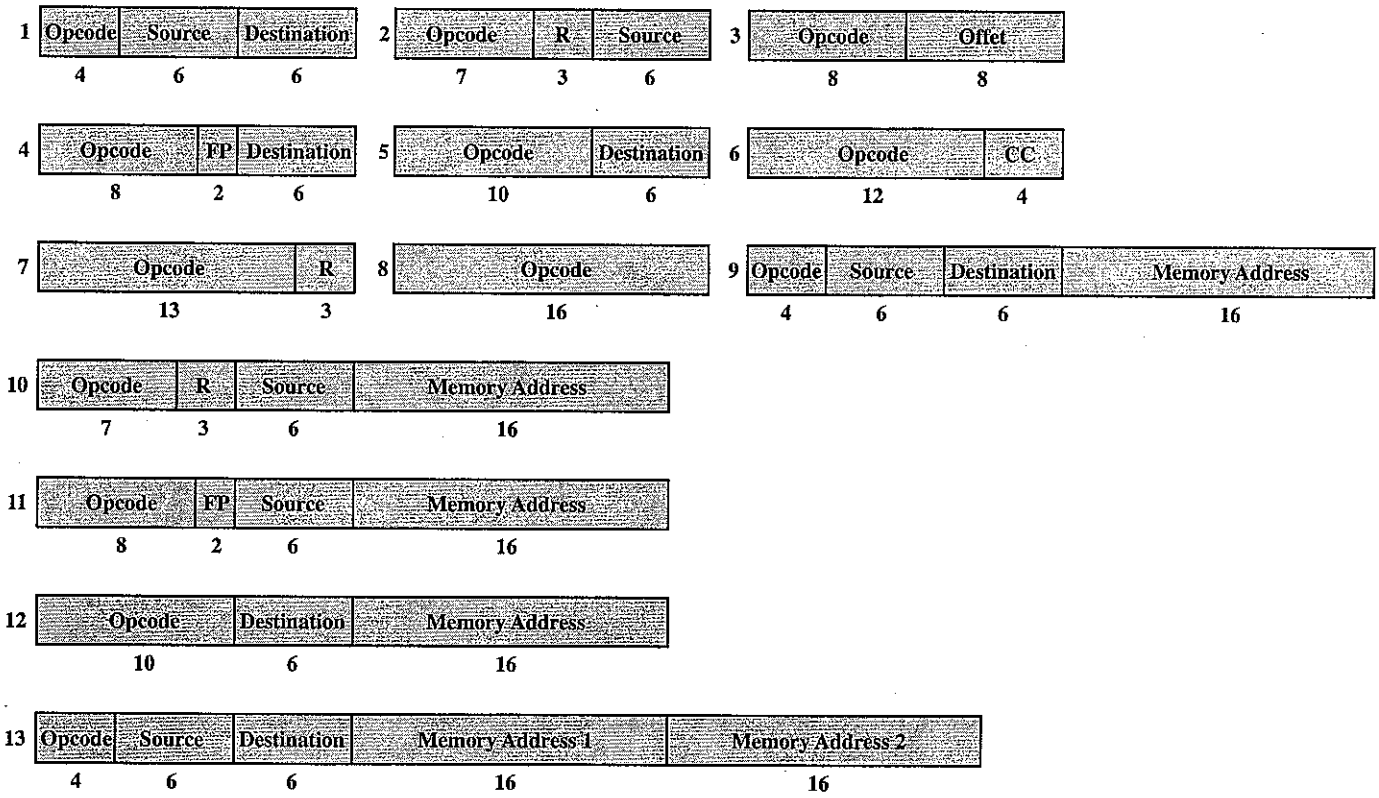
Factors

- number of addressing modes
  implicit or explicit
- number of operands
  majority 2 operands
- register vs. memory
  1. single register (accumulator) – implicit
  2. multiple registers
     4 bits → 16 registers
     5 bits → 32 registers
- number of register sets
  general-purpose
  specialized
  Ex. Index (Si,Di), counter (CX)
- address range
  direct addressing – limited
  displacement addressing – length of the address register
- addressing granularity
  byte or word



I = indirect bit

Figure 11.5 PDP-10 Instruction Format



Numbers below fields indicate bit length
Source and Destination each contain a 3-bit addressing mode field and a 3-bit register number
FP indicates one of four floating-point registers
R indicates one of the general-purpose registers
CC is the condition code field

Figure 11.6 Instruction Formats for the PDP-11