SYSTEM PERSPECTIVE ON DIAGNOSTIC TESTING

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Testing is performed for a variety of reasons—performance verification, experimentation, manufacturing assurance, diagnosis, process improvement, etc. The growing complexity of full-scale systems has outstripped our ability to provide detailed simulations for micro level diagnosis. When we have completed the experimentation and the verification through brass-board, we begin full scale engineering development. During this process we often redesign or include design features that allow us to have a high confidence that the part was manufactured correctly. For example, boundary scan may allow us to examine and verify every gate in a chip, or a test block on a board will allow us direct access to a number of devices on the board. System level diagnosis, however, is not addressed. In fact we go to great lengths to avoid it by incoming screening, chip test, board test, etc. Even 0.1% rejection at system delivery (because it fails some performance test) is unacceptable. Finding fault and fixing the system is expensive and time consuming, and it is better to avoid the problem all together. But—this is precisely the problem we give to the customer. We provide a full-up system, that after a certain number of operating hours fails and the customer has to repair it.

To understand why this becomes an expensive and time consuming problem, we can go back to manufacturing. Manufacturers include a great deal of micro level testing that becomes the basis for "system level testing". Next, they add some ad-hoc developed tests that localize to a subsystem that will be picked apart by minutia testing. The problem is massive computational resources are required to handle higher levels of complexity.

For example, suppose that we have a VLSI chip with 10,000 gates. If we consider the number of bridging faults, delay faults, and stuck-open faults, it is easy to have in excess of 50,000 defect sites to diagnose on the one chip. This is probably ideal for boundary scan operations, but this chip is one of four chips on a board with other components, and six boards make up the digitizer in a color radar that has 23 similar subsystems. Further, in order to trigger the boundary scan on the VLSI chip, we must assume more than 1,000 gates do their job getting our input signal to the chip and another 1,000 gates must do their job just to get the answer back to an output. With the combinations and permutations developed at this level of complexity it is not practical to attack the problem at the micro level. Improved technology eventually folds back into the system aggravating the problem.

From a system level approach, diagnosis will be taken to represent the process by which we localize a failure to a subset of elements that are consistent with the replacement of a single unit at the system level. Note that the term "system" is left to the user to define and it may be a fielded unit, a box in a shop, or a board on a special tester. In search of a less computationally intense process, we must build an analysis method that is hierarchical and examines functional capability. This latter approach we will call the system perspective.

The system perspective will allow us to quickly and efficiently localize failures, but it requires some re-thinking of the problem during design and manufacture to accommodate testing for system level diagnosis. It is not a replacement for the other types of testing that is performed. Nor is it just a "desirable" option, since users are demanding that the system perspective be built into new systems. Commercially, the scheduled airlines are developing the Portable Maintenance Access Terminal (PMAT) and the Onboard Maintenance System (OMS) to be first implemented on the Boeing 777. The military have developed two applicable specifications, MIL-STD-2165 for the establishment of testability programs and MIL-STD-1814 for the establishment of integrated diagnostic requirements.

While the customer is strengthening requirements, the industry has answered with a number of tools that allow us to explore, analyze, and make design recommendations. Such tools as STAMP, POINTER, STAT, IDSS, I-CAT, AI-TEST, and others are available and in use today. The more successful of these tools use an information flow modeling approach. This approach has been so successful, in fact, that the IEEE is in the process of standardizing the information flow model through its PAR 1232. The hierarchical nature of this approach can be noted by the fact that the modeling technique has been applied to a portable maintenance aid for the B-52 Environmental Control System, the development of an online performance fault monitoring system for a fuel-cell power plant, and the development of ATE for boards in the stores management system of the AV-8B.

It is now time to move the system perspective on diagnostic testing out of the experimental stage. Enough hard science has been accomplished that we can incorporate it as an engineering discipline in our new system development.

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